

INCREASING A REFRESH PERIOD IN A SEMICONDUCTOR MEMORY DEVICE

ABSTRACT OF THE DISCLOSURE

In one method according to an embodiment of the invention, a reference bitline is biased and a refresh period of a DRAM cell is increased. In one example of such a method, biasing the reference bitline includes applying a predetermined bias voltage. In a memory device according to one embodiment of the invention, a bias circuit includes a bias capacitor connected to a bitline and configured and arranged to receive a bias signal.